UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,846	07/20/2006	Ingrid Verbauwhede	UCLARF.004NP	3453

20995 7590 06/08/2010

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
TABLER, MATTHEW C	

ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
06/08/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jcartee@kmob.com
efiling@kmob.com
eOAPilot@kmob.com

Office Action Summary	Application No.	Applicant(s)	
	10/586,846	VERBAUWHEDE ET AL.	
	Examiner	Art Unit	
	MATTHEW C. TABLER	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-7,9-12 and 23-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-7,9-12 and 23-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to applicant's remarks filed on April 16th, 2010. Currently, claims 3-7, 9-12 and 23-27 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 3-7, 9-12 and 23-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Pilling (US Patent 6,573,775) filed on December 5th, 2001.

Regarding claim 3, Pilling shows a wave dynamic differential logic (Figure 7), comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs receive DATA & DATAB; CLK & CLKB), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs Q & QB), said differential logic cell configured to receive a precharge wave (CLK, CLKB) and/or a pre-discharge wave on said inverted inputs and non-inverted inputs (received at inputs) and to propagate said precharge wave and/or said pre-discharge wave from said inverted inputs and corresponding non-inverting inputs to said inverted logic outputs and said non-inverted logic outputs (clock

signals CLK and CLKB precharge the differential logic cell with Q13, Q14 and pre-discharge the cell through Q1).

Regarding claim 4, Pilling shows a wave dynamic differential logic (Figure 7), comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs receive DATA & DATAB; CLK & CLKB), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs Q & QB), and a pre-discharged logic cell (Q1) configured to receive a pre-discharge signal (CLKB) and, in response to said pre-discharge signal, to generate a pre-discharge wave to pre-discharge and propagate through said differential logic cell from said inverted inputs and non-inverted inputs to said inverted logic outputs and non-inverted logic outputs (Q1 discharges outputs OUTBM and OUTM) and/or a precharged logic cell configured to receive a precharge signal (Q13, Q14) and, in response to said precharge signal, to generate a precharge wave to pre-charge and propagate through said differential logic cell from said inverted inputs and non-inverted inputs to said inverted logic outputs and non-inverted logic outputs (Q13 and Q14 pre-charge outputs OUTBM and OUTM).

Regarding claim 5, Pilling shows a wave dynamic differential logic (Figure 7), comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs receive DATA & DATAB; CLK & CLKB), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs Q & QB), and a master-slave differential dynamic logic register (master 310a, slave 310b) configured to receive a precharge signal

(CLKB) and, in response to said precharge signal, to generate a pre-charge wave to pre-charge and propagate through said differential logic cell from said inverted inputs and non-inverted inputs to said inverted logic outputs and non-inverted logic outputs (clock signal pre-charges the outputs).

Regarding claim 6, Pilling shows a wave dynamic differential logic (Figure 7), comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs receive DATA & DATAB; CLK & CLKB), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs Q & QB), and a master-slave differential dynamic logic register (master 310a, slave 310b) configured to receive a pre-discharge signal (CLKB) and, in response to said pre-discharge signal, to generate a pre-discharge wave in response to said pre-discharge signal to pre-discharge and propagate through said differential logic cell from said inverted inputs and non-inverted inputs to said inverted logic outputs and non-inverted logic outputs (clock signal pre-discharges the outputs).

Regarding claim 7, Pilling shows a divided wave dynamic differential logic DPA-resistant logic circuit (Figure 7), comprising a first logic tree (master circuit 310) comprising a plurality of first logic tree inputs (inputs receive DATA & DATAB; CLK & CLKB) and a plurality of first logic tree outputs (OUTBM and OUTM) and configured to, during an evaluation phase (clock cycle), receive inverted input data and corresponding non-inverted input data on said first logic tree inputs (DATA & CLKB) and to produce first output data on said first logic tree outputs (OUTM), and a dual of said first logic tree (slave circuit 310b) comprising a plurality of dual logic tree inputs (DATA & CLKB) and a

plurality of dual logic tree outputs (OUTM) and configured to, during said evaluation phase (clock cycle), receive said inverted input data and said corresponding non-inverted input data on said dual logic tree inputs (receives inverted inputs DATA & DATAB) and produce inverted first output data on said dual logic tree outputs (Q and QB), said first logic tree and said dual of said first logic tree further configured to, during a precharge and/or pre-discharge phase (CLK and CLKB signals), receive a precharge wave and/or a pre-discharge wave on said first logic tree inputs and said dual logic tree inputs and propagate said precharge wave and/or pre-discharge wave to said first logic tree outputs and said dual logic tree outputs (Q1 and Q4 provide pre-discharge wave and Q13, Q14, Q16 and Q17 provide precharge wave).

Regarding claim 9, Pilling shows a wave dynamic differential logic (Figure 7), comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs receive DATA & DATAB; CLK & CLKB), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs Q & QB), and a master-slave differential dynamic logic register (master 310a, slave 310b) configured to receive a precharge wave and transmits on the pre-charge wave to pre-charge said differential logic cell (CLK and CLKB), the differential logic cell further configured to receive the precharge wave on said inverted inputs and non-inverted inputs and to propagate said pre-charge wave from said inverted inputs and corresponding non-inverting inputs to said inverted logic outputs and said non-inverted logic outputs (Q1 and Q4 provide pre-discharge wave and Q13, Q14, Q16 and Q17 provide precharge wave)..

Regarding claim 10, Pilling shows a wave dynamic differential logic (Figure 7), comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs receive DATA & DATAB; CLK & CLKB), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs Q & QB), and a differential dynamic logic register configured to receive a pre-charge signal (CLK and CLKB) and, in response to said pre-charge signal, to generate a pre-charge wave to pre-charge said differential logic cell (Q13 and Q14 charge the output nodes to VDD), the differential logic cell further configured to receive the precharge wave on said inverted inputs and non-inverted inputs (CLK and CLKB received by inputs) and to propagate said pre-charge wave from said inverted inputs and corresponding non-inverting inputs to said inverted logic outputs and said non-inverted logic outputs (Q1 and Q4 provide pre-discharge wave and Q13, Q14, Q16 and Q17 provide precharge wave)..

Regarding claim 11, Pilling shows a wave dynamic differential logic (Figure 7), comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs receive DATA & DATAB; CLK & CLKB), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs Q & QB), and a master-slave differential dynamic logic register (master 310a, slave 310b) configured to receive a pre-discharge wave (CLK and CLKB) and to transmits on the pre-discharge wave to pre-discharge said differential logic cell (310a), the differential logic cell further configured to receive the pre-discharge wave on said inverted inputs and non-inverted inputs (CLK and CLKB

received by inputs) and to propagate said pre-discharge wave from said inverted inputs and corresponding non-inverting inputs to said inverted logic outputs and said non-inverted logic outputs (Q1 and Q4 provide pre-discharge wave and Q13, Q14, Q16 and Q17 provide precharge wave)..

Regarding claim 12, Pilling shows a wave dynamic differential logic (Figure 7), comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs receive DATA & DATAB; CLK & CLKB), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs Q & QB), and a differential dynamic logic register (master 310a, slave 310b) configured to receive a pre-discharge signal and generate a pre-discharge wave to pre-discharge said differential logic cell (CLK and CLKB), the differential logic cell further configured to receive the pre-discharge wave on said inverted inputs and non-inverted inputs (CLK and CLKB received by inputs) and to propagate said pre-discharge wave from said inverted inputs and corresponding non-inverting inputs to said inverted logic outputs and said non-inverted logic outputs (Q1 and Q4 provide pre-discharge wave and Q13, Q14, Q16 and Q17 provide precharge wave)..

Regarding claim 23, Pilling shows positive logic (n-type transistors).

Regarding claim 24, Pilling shows positive logic (n-type transistors).

Regarding claim 25, Pilling shows positive logic (n-type transistors).

Regarding claim 26, Pilling shows positive logic (n-type transistors).

Regarding claim 27, Pilling shows said differential logic cell receives and propagates said precharge wave and/or said pre-discharge wave during a precharge and/or pre-discharge phase (CLK and CLKB clock cycle), and is further configured to, during an evaluation phase (clock cycle), receive differential data on said inverted inputs and said corresponding non-inverted inputs (inputs receive DATA & DATAB) and evaluate said differential data to produce differential output data on said inverted logic outputs and said non-inverted logic outputs (outputs Q and QB).

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW C. TABLER whose telephone number is (571)270-1567. The examiner can normally be reached on Monday through Friday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 277-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. C. T./
Examiner, Art Unit 2819

/James H. Cho/
Primary Examiner, Art Unit 2819

June 4, 2010